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TITLE: Nonvolatile memory cell with a floating gate  
at least partially located in a trench in a  
semiconductor substrate

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Abstract Paragraph - ABTX (1):

A floating gate (110) of a nonvolatile memory cell is formed in a trench (114) in a semiconductor substrate (220). A dielectric (128) covers the surface of the trench. The wordline (140) has a portion overlying the trench. The cell's floating gate transistor has a first source/drain region (226), a channel region (224), and a second source/drain region (130). The dielectric (128) is stronger against leakage near at least a portion of the first source/drain region (122) than near at least a portion of the channel region. The stronger portion (128.1) of the additional dielectric improves data retention without increasing the programming and erase times if the programming and erase operations do not rely on a current through the stronger portion. Additional dielectric (210) has a portion located below the top surface of the substrate between the trench and a top part of the second source/drain region (130). The second source/drain region has a part located below the additional dielectric and meeting the trench. The additional dielectric can be formed with shallow trench isolation technology. The additional dielectric reduces the capacitance between the second source/drain region (130) and the floating gate.

Title - TTL (1):

Nonvolatile memory cell with a floating gate at least partially located in

a trench in a semiconductor substrate

Continuity Related Application Date - RLFD (2):

20020919

Summary of Invention Paragraph - BSTX (3):

[0002] FIG. 1 illustrates a nonvolatile memory cell with a floating gate 110 located in a trench 114 formed in a semiconductor substrate. The cell is obtained by adapting a trench capacitor DRAM (dynamic random access random memory) fabrication process. See U.S. Pat. No. 5,932,908 issued Aug. 3, 1999 to Noble, entitled "TRENCH EPROM", incorporated herein by reference.

Trench 114 extends through a well 118 doped P- and a well 122 doped N+, to a region 126 doped P-. Dielectric 128 lines the trench. The capacitance of floating gate 110 is dominated by the capacitance between the floating gate and the N well 122.

Summary of Invention Paragraph - BSTX (4):

[0003] Floating gate 110 serves as the gate of a vertical FET (field effect transistor). The channel of this transistor is located in P well 118. The source/drain regions are provided by N well 122 and an N+ diffusion region 130 located at the top of the trench.

Summary of Invention Paragraph - BSTX (6):

[0005] The cell can be written by storing either a positive or a negative charge on the floating gate. The negative charge is stored by the channel hot electron injection. In this operation, bit line region 150 is grounded. Wordline 140 is brought up to some voltage VDD, turning on the select transistor. N well 122 is at 6V. Due to the capacitive coupling between the N well 122 and the floating gate, the floating gate voltage is raised, turning on the vertical FET. Hot electrons generated in the channel of the vertical FET are injected into the floating gate.

Summary of Invention Paragraph - BSTX (10):

[0009] One advantage of forming the floating gate in the trench is a small cell area. Another advantage is a high capacitive coupling between the floating gate and the N well 122 relative to the total floating gate capacitance. This high capacitive coupling efficiency (high capacitive coupling relative to the total floating gate capacitance) is easier to achieve than an efficient coupling between the floating and control gates in some non-trench structures, as described in the U.S. Pat. No. 5,932,908.

Summary of Invention Paragraph - BSTX (11):

[0010] Another advantage is a close relationship to trench capacitor DRAM fabrication processes. This relationship facilitates integration of the floating gate memory and trench capacitor DRAM on one chip.

Summary of Invention Paragraph - BSTX (14):

[0012] In some embodiments of the invention, a floating gate of a nonvolatile memory cell is formed in a trench as in FIG. 1, but the wordline has a portion overlying the trench. See FIG. 2A for example. This wordline positioning offers much flexibility in the memory layout. For example, the region 130 in FIG. 2A can be extended around the floating gate to increase the vertical FET channel width. A large vertical FET channel width reduces the cell's programming time if the cell is programmed by channel hot electron injection. The cell reading time can also be reduced due to a larger current through the cell.

Summary of Invention Paragraph - BSTX (15):

[0013] In some embodiments of the present invention, the dielectric lining the trench is stronger against leakage near one of the source/drain regions of the floating gate transistor than near the channel region. For example, in FIG. 2A, the dielectric lining the trench has a bottom portion 128.1 near the bottom source/drain region 226 and has a portion 128.2 near the channel region. Bottom portion 128.1 is stronger against leakage than the portion

128.2.

"Stronger" means the leakage per unit area is smaller at a given voltage across the dielectric. As is well known, small leakage improves data retention but undesirably increases the programming and erase times (or voltages). If the memory is not programmed or erased through the bottom source/drain region, the stronger dielectric near this region improves data retention without increasing the programming and erase times or voltages.

Summary of Invention Paragraph - BSTX (16):

[0014] In some embodiments, additional dielectric is provided between the trench and a top part of a source/drain region of the floating gate transistor. For example, in FIG. 2A, the additional dielectric is a portion of dielectric 210 extending below the top surface of the substrate between the trench 114 and the top part of source/drain region 130. Region 130 passes under the dielectric 210 to meet the trench 114. The additional dielectric reduces the capacitance between the region 130 and the floating gate. The additional dielectric can be part of a field dielectric layer, i.e. the layer that isolates active areas of the integrated circuit from each other.

Summary of Invention Paragraph - BSTX (17):

[0015] The features described above can be used separately or in combination. For example, some embodiments have a wordline arranged as in FIG. 1 (not overlying the trench), but the dielectric lining the trench is made stronger near a source/drain region of the floating gate transistor (like dielectric 128.1, 128.2 in FIG. 2A). In some embodiments with the stronger dielectric, a select transistor is absent. Also, the additional dielectric between the trench and a top part of a source/drain region (like dielectric 210 in FIG. 2A) can be provided in memories in which the wordline does not overlie the trench, and in memories that do not have a select transistor.

Detail Description Paragraph - DETX (3):

structure is planarized, with the trench oxide protruding above the substrate 220. Pad oxide 1010 is removed in this etch.

Detail Description Paragraph - DETX (55):

[0085] N type regions 234, 238 (FIGS. 2A, 28A) are created by a series of ion implantation steps to create the isolated P well 224, as described in the aforementioned U.S. Pat. No. 6,355,524. Region 238 is not shown in FIG. 28A and the subsequent figures.

Detail Description Paragraph - DETX (56):

[0086] A P type dopant (e.g. boron) can be implanted into substrate 220 to adjust the doping concentration in P well 224. This implant adjusts the threshold voltages of the select and floating gate transistors of the memory cells. This can be a blanket implant, or a series of implantation steps with photoresist masks for independent adjustment of the threshold voltages of different transistors of the memory cells and possibly of other transistors (not shown) in the integrated circuit.

Detail Description Paragraph - DETX (58):

[0088] Source line regions 130 and bitline regions 150 can now be doped using conventional fabrication techniques. LDD (lightly doped drain), DDD (double diffused drain), or other doping profiles can be formed as desired for the select transistors. In one embodiment, an LDD doping profile is formed both at the source line regions and at the bitline regions for the select transistors as follows. The wafer is coated with photoresist 2804 (FIG. 28A). The resist is patterned to expose the source line regions. FIG. 28C shows the top view of the structure. FIG. 28A shows the cross section along the plane "28A-28A" marked in FIG. 28C (this is the same plane as the plane "A-A" in FIG. 2B). FIG. 28B shows the cross section along the plane "28B-28B" of FIG. 28C

(this plane is marked "D-D" in FIG. 2B). An N type dopant (e.g. phosphorous) is implanted to dope the source line regions N-. Resist 2804 is removed, and a photoresist layer 2904 (FIGS. 29A, 29B, 29C) is formed on top of the wafer. FIG. 29C shows the top view of the structure. FIG. 29A shows the cross section along the plane "29A-29A" of FIG. 29C (plane "A-A" in FIG. 2B). FIG. 29B shows the cross section along the plane "29B-29B" of FIG. 29C (plane "D-D" in FIG. 2B). Resist 2904 is patterned to expose the bitline regions 150. An N type dopant is implanted to dope the bitline regions N-. Resist 2904 is removed, and spacers 254 are formed by a conformal deposition and an anisotropic etch of silicon dioxide or some other dielectric. If gate oxide 260 remains on the active areas not covered by wordline 140, oxide 260 can be removed during the etch of dielectric 254.

Detail Description Paragraph - DETX (59):

[0089] Then an N+ implant is performed into the source line regions 130 and bitline regions 150.

Detail Description Paragraph - DETX (60):

[0090] In the embodiment just described, the N-doping of source line regions 130 and bitline regions 150 is performed separately because it may be desirable to dope the bitline regions more heavily but make them shallower than the source line regions. The source line regions are doped more lightly to reduce hot electron generation in the floating gate transistor channel in read operations. In other embodiments, the regions 130, 150 are doped N- in the same implantation step.

Detail Description Paragraph - DETX (62):

[0092] In some embodiments, the doping step of FIGS. 25A-25C is omitted. The source line dopant implanted at the stage of FIGS. 28A-28C and the subsequent stages diffuses into the substrate and reaches the deep

**trench** 114

under the STI **trench** 270 (under the STI oxide 210).

Detail Description Table CWU - DETL (2):

2TABLE 2 D1 (AA width in WL (wordline) direction at edges of 0.18 .mu.m regions 130 and at bitline region 150) D2 (distance between AA and deep **trench** 114 at edges 0.11 .mu.m of regions 130 and at regions 150) D3 (deep **trench** 114 width in WL direction) 0.20 .mu.m D4 (distance between deep **trench** 114 and the nearest 0.12 .mu.m active area in the adjacent column) D5 (distance between adjacent deep **trenches** 114 in 0.18 .mu.m adjacent pairs of rows) D6 (distance between wordline 140 and the farthest edge 0.24 .mu.m of **trench** 114 in a memory cell) D7 (width of WL 140) 0.18 .mu.m D8 (distance between WLs 140 in one pair of rows) 0.26 .mu.m D9 (distance between WL 140 and bitline contact area in 0.08 .mu.m bitline region 150) Cell area (D1 + D2 + D3 + D4) \* (D5/2 + D6 + D7 + D8/2) = 0.3904 .mu.m.sup.2

Claims Text - CLTX (1):

1. An integrated circuit comprising a first nonvolatile memory cell, the integrated circuit comprising: a semiconductor substrate having a top surface and a **trench** formed in the top surface; a dielectric on a surface of the **trench**; a conductive floating gate at least partially located in the **trench**; wherein the first nonvolatile memory cell comprises a first field effect transistor (FET) whose conductivity is at least partially controlled by the floating gate, and comprises a second FET for controlling access to the first FET; wherein the substrate comprises: a first semiconductor region of a first conductivity type adjacent to the **trench** and providing a first source/drain region for the first FET; a second semiconductor region of a second conductivity type adjacent to the **trench** above the first semiconductor region and providing a channel region for the first FET; a third semiconductor region

of the first conductivity type, wherein at least a portion of the third semiconductor region lies adjacent to the trench above the second semiconductor region and provides a second source/drain region for the first FET, wherein the third semiconductor region also provides a source/drain region for the second FET; a fourth semiconductor region of the second conductivity type adjacent to the third semiconductor region and providing a channel region for the second FET; and a fifth semiconductor region of the first conductivity type adjacent to the fourth semiconductor region and providing a source/drain region for the second FET; wherein the integrated circuit further comprises a conductive member having a portion overlying the trench, wherein the conductive member provides a gate for the second FET.

Claims Text - CLTX (3):

3. The integrated circuit of claim 1 wherein the third semiconductor region curves around the trench adjacent to the trench.

Claims Text - CLTX (4):

4. The integrated circuit of claim 1 wherein the first and second source/drain regions of the first FET and the channel region of the first FET curve around the trench.

Claims Text - CLTX (5):

5. The integrated circuit of claim 4 wherein the first and second semiconductor regions laterally surround the trench.

Claims Text - CLTX (6):

6. The integrated circuit of claim 1 wherein the entire third semiconductor region is located on one side of the trench.

Claims Text - CLTX (7):

7. The integrated circuit of claim 5 wherein the third, fourth and fifth semiconductor regions are entirely located on one side of the trench.

Claims Text - CLTX (8):

8. The integrated circuit of claim 1 further comprising a dielectric region



having at least a portion extending below the top surface of the substrate  
between the trench and a top part of the third semiconductor region,  
wherein  
the third semiconductor region has a part located below said portion  
of the  
dielectric region and meeting the trench.

Claims Text - CLTX (9):

9. The integrated circuit of claim 8 wherein the dielectric region has a portion extending below the top surface of the substrate and overlapping the trench.

Claims Text - CLTX (10):

10. The integrated circuit of claim 1 wherein the dielectric on the surface of the trench is stronger against leakage adjacent at least a portion of the first semiconductor region than adjacent at least a portion of the second semiconductor region.

Claims Text - CLTX (12):

12. The integrated circuit of claim 1 wherein all of the floating gate is in the trench.

Claims Text - CLTX (14):

14. The integrated circuit of claim 1 comprising a plurality of nonvolatile memory cells, the first nonvolatile memory cell being one of the plurality;  
wherein the semiconductor substrate comprises, for each cell, a trench formed in the top surface of the substrate; wherein the integrated circuit comprises,  
for each cell, a dielectric on the surface of the respective trench and a floating gate at least partially located in the respective trench;  
wherein  
each cell comprises a respective first FET whose conductivity is at least partially controlled by the respective floating gate, and comprises a respective second FET for controlling access to the respective first FET;  
wherein the substrate comprises, for each cell: a first semiconductor region of a first conductivity type adjacent to the respective trench and

providing a first source/drain region for the first FET of the cell; a second semiconductor region of a second conductivity type adjacent to the respective **trench** above the respective first semiconductor region and providing a channel region for the first FET of the cell; a third semiconductor region of the first conductivity type, wherein at least a portion of the third semiconductor region lies adjacent to the respective **trench** above the respective second semiconductor region and provides a second source/drain region for the first FET of the cell, wherein the third semiconductor region also provides a source/drain region for the second FET of the cell; a fourth semiconductor region of the second conductivity type adjacent to the respective third semiconductor region and providing a channel region for the second FET of the cell; and a fifth semiconductor region of the first conductivity type adjacent to the respective fourth semiconductor region and providing a source/drain region for the second FET of the cell; wherein the integrated circuit further comprises a plurality of wordlines, each wordline being for selecting a subset of the memory cells, wherein each wordline has portions overlying the **trenches** of the corresponding subset of the memory cells and provides gates for the second FETs of the corresponding subset of the memory cells, said conductive member being one of the wordlines.

Claims Text - CLTX (18):

18. The integrated circuit of claim 17 wherein in each column of the memory cells, all of the third, fourth and fifth semiconductor regions are entirely located on one side of an area occupied by the **trenches**.

Claims Text - CLTX (19):

19. A method for fabricating the integrated circuit of claim 1, the method comprising: forming the **trench** in the top surface of the semiconductor

substrate; forming the dielectric on the surface of the trench;  
forming the  
conductive floating gate at least partially located in the trench;  
and forming  
the conductive member.

Claims Text - CLTX (20):

20. An integrated circuit comprising a nonvolatile memory cell,  
the  
integrated circuit comprising: a semiconductor substrate having a top  
surface  
and a first trench formed in the top surface; a dielectric on a  
surface of the  
first trench; a conductive floating gate at least partially located  
in the  
first trench; wherein the nonvolatile memory cell comprises a first  
field  
effect transistor (FET) whose conductivity is at least partially  
controlled by  
the floating gate; wherein the substrate comprises: a first  
semiconductor  
region of a first conductivity type adjacent to the first trench and  
providing  
a first source/drain region for the first FET; a second  
semiconductor region  
of a second conductivity type adjacent to the first trench above the  
first  
semiconductor region and providing a channel region for the first  
FET; a third  
semiconductor region of the first conductivity type, wherein at least  
a portion  
of the third semiconductor region lies adjacent to the first trench  
above the  
second semiconductor region and provides a second source/drain region  
for the  
first FET; wherein the integrated circuit further comprises a  
dielectric  
region having at least a portion extending below the top surface of  
the  
substrate between the first trench and a top part of the third  
semiconductor  
region, wherein the third semiconductor region has a part located  
below said  
portion of the dielectric region and meeting the first trench.

Claims Text - CLTX (21):

21. The integrated circuit of claim 20 wherein the dielectric  
region has a  
portion extending below the top surface of the substrate and  
overlapping the

first trench.

Claims Text - CLTX (23):

23. The integrated circuit of claim 20 wherein the dielectric on the surface of the first trench is stronger against leakage adjacent at least a portion of the first semiconductor region than adjacent at least a portion of the second semiconductor region.

Claims Text - CLTX (25):

25. The integrated circuit of claim 20 wherein all of the floating gate is in the first trench.

Claims Text - CLTX (27):

27. A method for fabricating the integrated circuit of claim 20, the method comprising: forming the first trench in the top surface of the semiconductor substrate; forming the dielectric on the surface of the first trench; forming the floating gate at least partially located in the first trench; and forming the dielectric region.

Claims Text - CLTX (30):

30. The method of claim 27 wherein forming at least said portion of the dielectric region comprises: forming a second trench in the top surface of the substrate; and filling the second trench with dielectric.

Claims Text - CLTX (31):

31. The method of claim 30 wherein the second trench is not as deep as the first trench.

Claims Text - CLTX (32):

32. The method of claim 30 further comprising, after forming the second trench but before filling the second trench with the dielectric, introducing a dopant into a bottom surface of the second trench adjacent to the first trench to dope at least a portion of the third semiconductor region.

Claims Text - CLTX (33):

33. An integrated circuit comprising: a semiconductor substrate

having a top surface and a trench formed in the top surface; a first dielectric on a surface of the trench; a conductive floating gate at least partially located in the trench; wherein the nonvolatile memory cell comprises a first field effect transistor (FET) comprising said floating gate; wherein the substrate comprises: a first semiconductor region of a first conductivity type adjacent to the trench and providing a first source/drain region for the first FET; a second semiconductor region of a second conductivity type adjacent to the trench above the first semiconductor region and providing a channel region for the first FET; a third semiconductor region of the first conductivity type, wherein at least a portion of the third semiconductor region lies adjacent to the trench above the second semiconductor region and provides a second source/drain region for the first FET; wherein the first dielectric comprises a first portion and a second portion, the first portion being stronger against leakage than the second portion, wherein at least part of the first semiconductor region is adjacent to the first portion of the first dielectric, and at least part of the second semiconductor region is adjacent to the second portion of the first dielectric.

Claims Text - CLTX (40):

40. A method for fabricating the integrated circuit of claim 33, the method comprising: forming the trench in the top surface of the semiconductor substrate; forming the first and second portions of the first dielectric on the surface of the trench; and forming the floating gate at least partially located in the trench.